

What is Claimed is:

1        1.    During the testing of the operation of processing  
2    unit, a system for identifying the occurrence of a program  
3    code start point condition in the pipeline flattener, the  
4    system comprising:  
5        timing trace apparatus responsive to signals from the  
6    processor unit, the timing trace apparatus generating a  
7    timing trace stream;  
8        program counter trace apparatus responsive to signals  
9    from the processing unit, the program counter trace  
10   apparatus generating a program counter trace stream; and  
11        synchronization apparatus applying periodic signals to  
12   the timing trace apparatus and to the program counter trace  
13   apparatus, the periodic signals resulting in periodic sync  
14   markers in the timing trace stream and in the program  
15   counter trace stream.  
16        wherein the program counter trace apparatus is  
17   responsive to a program code start point signal, the  
18   program counter trace apparatus generating a sync marker  
19   signal group identifying the occurrence of the program code  
20   start point signal and relating the beginning of program  
21   code execution to the timing trace stream and to the  
22   program code execution.  
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1        2. The system as recited in claim 1 wherein the  
2 marker signal group includes a program counter address, a  
3 timing index and a periodic sync ID.

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5        3. The system as recited in claim 1 further  
6 comprising:

7        data trace apparatus responsive to signals from the  
8 processing unit, the data trace apparatus generating a data  
9 trace stream, wherein the periodic signals are applied to  
10 the data trace apparatus resulting in periodic sync markers  
11 in the data trace stream; and

12        a host processing unit, the host processing unit  
13 responsive to the timing trace stream, the program counter  
14 trace stream and the data trace stream, the host processing  
15 unit reconstructing the processing activity of the  
16 processing unit from the trace streams.

17        4. The method for communicating an occurrence of a  
18 program code start point signal from a target processor  
19 unit to a host processing unit after return from an  
20 interrupt service routine, the method comprising:

21        generating a timing trace stream, a program counter  
22 trace stream, and data trace stream, and

23        in the program counter trace stream, including a  
24 program code start point sync marker signal group  
25 indicating an occurrence of a program code start point  
26 signal and relating the signal occurrence to the data trace  
27 stream and to the timing trace stream.

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2       5.   The method as recited in claim 4 further  
3 including:

4       including periodic sync markers in the timing trace  
5 stream and in the program counter trace stream; and

6       including in the program code sync marker reference to  
7 a periodic sync marker.

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9       6.   In a processing unit test environment wherein a  
10 target processor transmits a plurality of trace streams to  
11 a host processing unit, a program code start point sync  
12 marker signal group in a trace signal stream, the marker  
13 signal group comprising:

14       indicia of the occurrence of a program code start  
15 point signal;

16       indicia of the relationship of the occurrence of the  
17 program code start point signal to the target processor  
18 clock; and

19       indicia of the relationship of the occurrence of the  
20 program code start point signal to the target processor  
21 program execution.

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23       7.   In a target processing unit generating trace test  
24 signals for transfer to a host processing unit, a program  
25 counter trace generation apparatus comprising:

26       sync marker assembly apparatus, the sync marker  
27 assembly apparatus including:

1           a storage unit;  
2           a decoder unit responsive to a program code start  
3 point signal for storing an indicia of the program code  
4 start point signal in the storage unit, the decoder unit  
5 generating a control signal;  
6           a gate unit having a timing index, a periodic  
7 sync signal, and a program counter address, the gate unit  
8 storing the timing index, the periodic sync signal and the  
9 program counter address in the storage unit in response to  
10 the control signal; and  
11           a FIFO unit, the storage unit transferring the  
12 stored signals to the FIFO unit in the form of a program  
13 code start point sync marker.

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15       8.   The program counter trace apparatus as recited in  
16 claim 7 responsive to a selected control signal for  
17 transferring the program code start point sync marker in  
18 the FIFO unit to an output port of the target processor.

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20       9.   The program counter trace apparatus as recited in  
21 claim 8 wherein the apparatus can form a periodic sync  
22 marker in response to a periodic sync signal.

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24       10.  The program counter trace apparatus as recited in  
25 claim 9 wherein the program code start point signal  
26 indicates the change from a first instruction code sequence

1 to a second instruction code sequence exiting the pipeline  
2 flattener.

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4 11. The program counter trace apparatus as recited in  
5 claim 10 wherein the first instruction code sequence is an  
6 interrupt service routine code and the second instruction  
7 sequence is a program code.

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